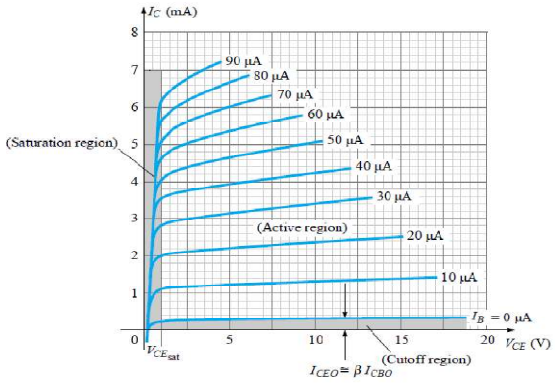
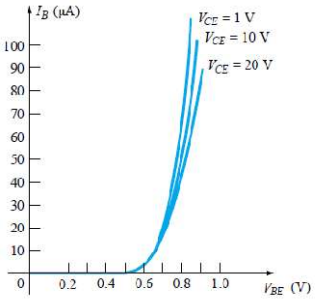
(Session-2018-19)

Current Mirror circuit

Common-Emitter Characteristics



Output Characteristics



Input Characteristics

Fundamental

- Biasing in integrated-circuit design is based on the use of constant-current sources.
- On an IC chip with a number of amplifier stages, a constant dc current (called a **reference current**) is generated at one location and is then replicated at various other locations for biasing the various amplifier stages through a process known as **current steering**.

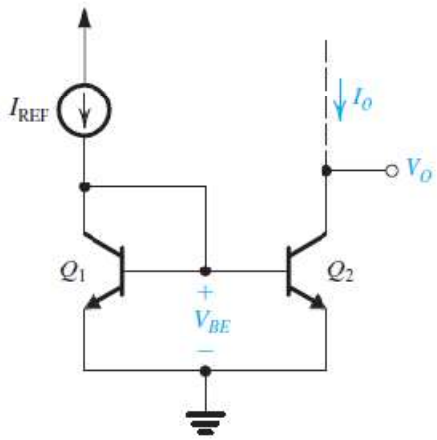
- This approach has the advantage that the effort expended on generating a predictable and stable reference current, usually utilizing a precision resistor external to the chip or a special circuit on the chip, need not be repeated for every amplifier stage.
- The bias currents of the various stages track each other in case of changes in power-supply voltage or in temperature.

BJT Circuits as current mirror

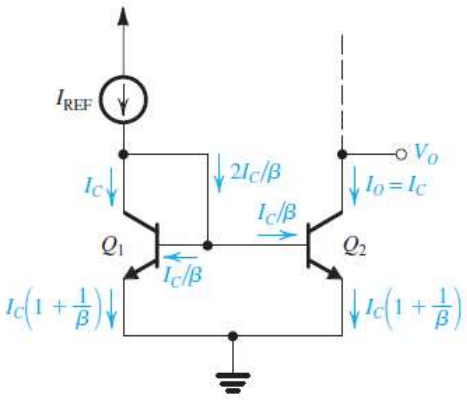
Diode equation; as Q1 is behaving as diode but it also inherits property of transistor.

$$I = I_0\left(e^{\frac{qV}{kT}} - 1\right)$$

V is replaced by V_{BE}



$$I_{REF} = I_C + 2I_C/\beta = I_C\left(1 + \frac{2}{\beta}\right)$$

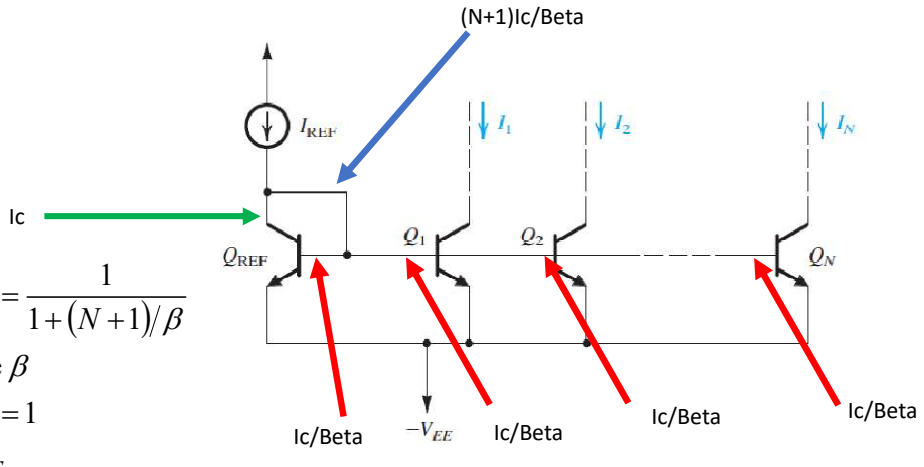


Finally, since $I_O - I_C$, the current transfer ratio can be found as

$$\frac{I_O}{I_{REF}} = \frac{I_C}{I_C\left(1+\frac{2}{\beta}\right)} = \frac{1}{1+\frac{2}{\beta}}$$

Note that as β approaches ∞, I_O / I_{REF} approaches the nominal value of unity. For typical values of β, however, the error in the current transfer ratio can be significant. For instance, β = 100 results in a 2% error in the current transfer ratio. Furthermore, the error due to the finite β increases as the nominal current transfer ratio is increased.

Consider with *N*-output current mirror.



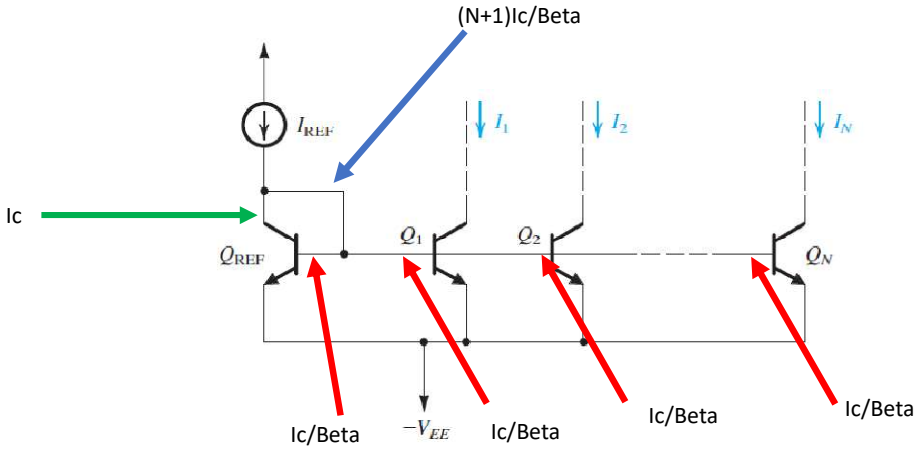
$$I_o / I_{REF} = \frac{1}{1+(N+1)/\beta}$$

With large β

$$I_o / I_{REF} = 1$$

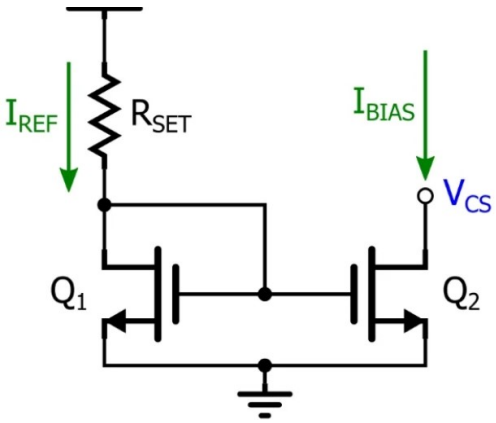
$$I_o = I_{REF}$$

Set I_{REF}

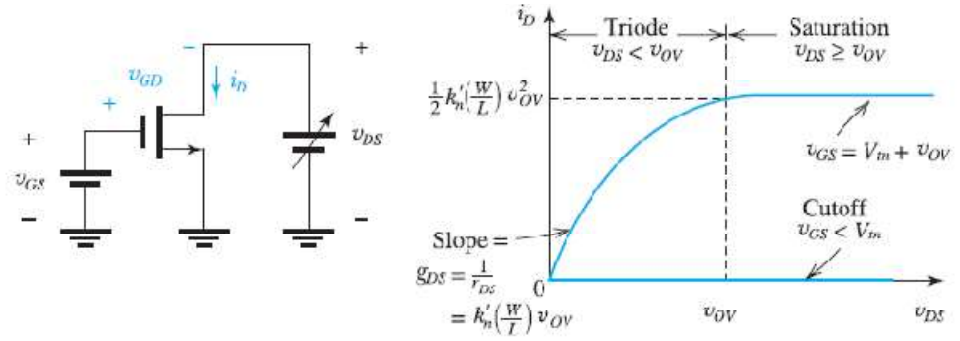


Current mirror circuit using FET

- A **current mirror** is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading.



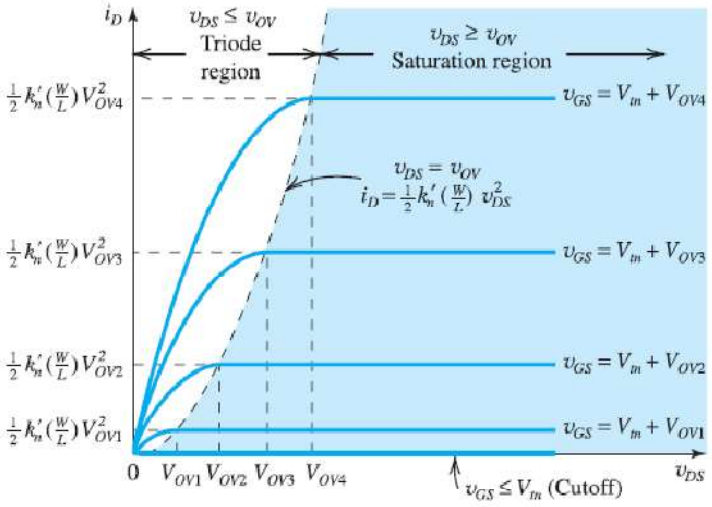
Fundamental concept behind current mirror



- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Fundamental concept behind current mirror contd..

Vov=Overdrive voltage

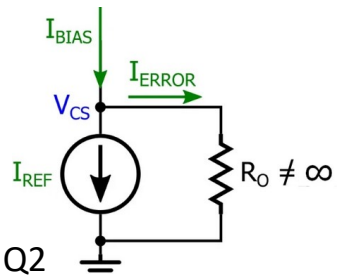


The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor.

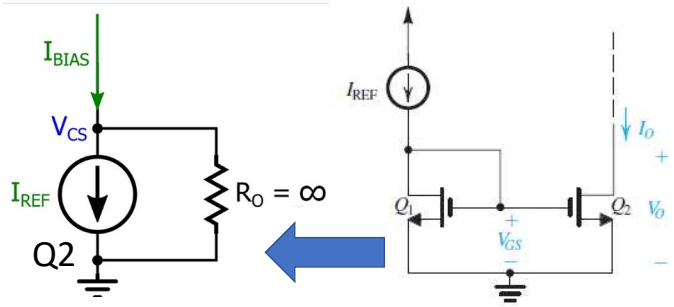
Just for student's understanding

- As you can see, the drain of Q_1 is shorted to its gate. This means that $V_G = V_D$, and thus $V_{GD} = 0$ V. So, is Q_1 in cutoff, the triode region, or the saturation region? It can't be in cutoff, because if no current were flowing through the channel, the gate voltage would be at V_{DD}, and thus V_{GS} would be greater than the threshold voltage V_{TH} (we can safely assume that V_{DD} is higher than V_{TH}). This means Q_1 will always be in saturation (also referred to as "active" mode), because $V_{GD} = 0$ V, and one way of expressing the condition for MOSFET saturation is that V_{GD} must be less than V_{TH}.
- If we recall that no steady-state current flows into the gate of a MOSFET, we can see that the reference current I_{REF} will be the same as Q_1's drain current. We can customize this reference current by choosing an appropriate value for R_{SET}. So what does all this have to do with Q_2? Well, the drain current of a MOSFET in saturation is influenced by the width-to-length ratio of the channel and the gate-to-source voltage.

- Now notice that both FETs have their sources tied to ground and that their gates are shorted together—in other words, both have the same gate-to-source voltage. Thus, if we assume that both devices have the same channel dimensions, their drain currents will be equal, *regardless of the voltage at the drain of Q_2*. This voltage is labeled V_{CS}, meaning the voltage across the current-source component; this helps to remind us that Q_2, like any well-behaved current source, generates a bias current that is not affected by the voltage across its terminals. Another way to say this is that Q_2 has infinite output resistance:



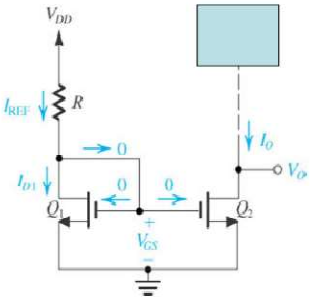
Practical



Ideal

Mathematical Fundamental for current mirror

Constant current source:



➔ Current mirror

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

Assuming Q_1, Q_2 have same properties (k_n'),

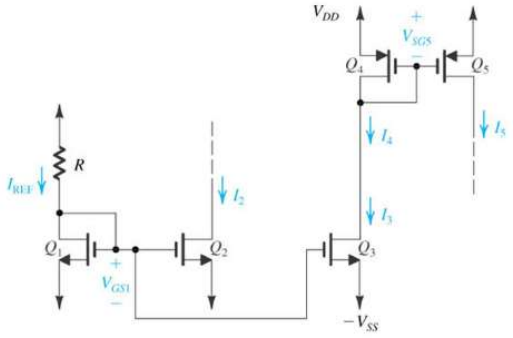
$$I_O = I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_{tn})^2$$

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

Limitation on V_o? $V_O \geq V_{GS} - V_t$

Example

(Without r_0 consideration)



$$I_2 = I_{REF}\frac{(W/L)_2}{(W/L)_1}$$

$$I_3 = I_{REF}\frac{(W/L)_3}{(W/L)_1}$$

$$I_3 = I_4$$

$$I_5 = I_4\frac{(W/L)_5}{(W/L)_4}$$

Current-steering circuits: current source (Q_5), current sink (Q_2)